(6 pages) **Reg. No. :** .....

Code No. : 30944 E **Sub. Code : FECS 11**

B.Sc. (CBCS) DEGREE EXAMINATION, NOVEMBER 2024.

First Semester

Computer Science

Elective – DIGITAL LOGIC FUNDAMENTALS

(For those who joined in July 2024 onwards)

Time : Three hours Maximum : 75 marks

PART A — (10 × 1 = 10 marks)

Answer ALL questions.

Choose the correct answer :

1. Which of the following is Natural number?

   (a) 3.5 (b) 7

   (c) 0 (d) –2

2. Integer numbers set is denoted by which letter?

   (a) N (b) W

   (c) Q (d) Z

3. Which of the following combinations of logic gates can decode binary 1101?

   (a) One 4-input AND gate

   (b) One 4-input AND gate, one inverter

   (c) One 4-input AND gate, one OR gate

   (d) One 4-input NAND gate, one inverter

4. In a combinational circuit, the output at any time depends only on the ———— at that time.

   (a) Voltage (b) Intermediate values

   (c) Input values (d) Clock pulses

5. In a sequential circuit, the output at any time depends only on the input values at that time.

   (a) Past output values

   (b) Intermediate values

   (c) Both past output and present input

   (d) Present input values

6. All logic operations can be obtained by means of ————.

   (a) AND and NAND operations

   (b) OR and NOR operations

   (c) OR and NOT operations

   (d) NAND and NOR operations

7. The truth table for an S-R flip-flop has how many VALID entries?

(a) 1 (b) 2

(c) 3 (d) 4

8. When both inputs of a J-K flip-flop cycle, the output will ————————.

(a) Be invalid (b) Change

(c) Not change (d) Toggle

9. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?

(a) Tristate (b) End around

(c) Universal (d) Conversion

10. How can parallel data be taken out of a shift register simultaneously?

(a) Use the Q output of the first FF

(b) Use the Q output of the last FF

(c) Tie all of the Q outputs together

(d) Use the Q output of each FF

PART B — ($5 \times 5 = 25$ marks)

Answer ALL questions, choosing either (a) or (b).
Each answer should not exceed 250 words.

11. (a) Convert the following:

Decimal Number 4097.188 into Binary Number.

Or

(b) Describe in brief The ASCII Code with example.

12. (a) Explain in detail about Duality Theorem with example.

Or

(b) Show the Logic Circuit for this Boolean Expression $Y(A\overline{B})(AB)$.

13. (a) Enumerate in detail about 8 to 1 Multiplexers with Logic Circuit and Truth Table.

Or

(b) Summarize in detail about BCD-TO-DECIMAL Decoder with neat diagram.

14. (a) Illustrate in detail about JK Master-Slave Flip Flops with Logic Diagram and Truth Table.

Or

(b) Illuminate in brief about Edge-triggered D Flip Flops with Logic Diagram and Truth Table.

15. (a) Relate in brief about Universal Shift Register with Logic Diagram and Truth Table.

Or

(b) Plan in detail about Serial In – Parallel Out with Logic Diagram and Truth Table.

PART C — ($5 \times 8 = 40$ marks)

Answer ALL questions, choosing either (a) or (b).
Each answer should not exceed 600 words.

16. (a) Elucidate in brief about The OR and AND Gate with its Logic Diagram and Truth table.

Or

(b) Convert the following

(i) Decimal Number $(193.3)_{10}$ to an Octal Number and Binary

(ii) Octal Number $(7765)_8$ to Decimal Number

(iii) Hexadecimal Number $(5C8)_{16}$ to an Binary

(iv) Octal Number $(1723)_8$ to Binary Number.

17. (a) Obtain the Canonical sum of product form of the function $Y(A, B, C) = A + BC$.

Or

(b) Simplify the following expression using the Karnaugh Map for the 4 variables A, B, C and D $Y = m_1 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{12} + m_{13}$.

18. (a) Paraphrase in brief about 1-OF-10 Decoder with Logic Circuit and Truth-Table.

Or

(b) Infer in detail about 2's Compliment Representation with example.

19. (a) Clear up in brief about Edge-triggered RS Flip Flops with Logic Diagram and Truth Table.

Or

(b) Point out in detail about RS Flip Flop with Logic Diagram and Truth Table.

20. (a) Analyze in brief about Serial In – Serial Out with Logic Diagram and Truth Table.

Or

(b) Illustrate in detail about Parallel In – Parallel Out with Logic Diagram and Truth Table.

———————